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Hardware Implementation of Battery Monitoring System Controller for Underwater Vehicles

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Abstract

Recent times design, development and testing of unmanned underwater vehicles for various civil and military missions have been enhanced. In underwater vehicle batteries are the main source of power supply to other subsystems. Monitoring of these batteries is an important activity to be performed by Battery Management System (BMS). It reduces the damage incurred in the various subsystems due to abnormal operating conditions and reflected voltage changes of the battery cells. Hence, the main objective of this paper is an implementation of the BMS controller in FPGA. The FPGA is the better choice to interface various sensors and ADC to PC to acquire the data for further processing. The total voltage is the cumulative voltage of the cells and is fed to the ADC through a signal conditioning circuit. The BMS controller is implemented in Verilog HDL using the Xilinx ISE design suite and validated using on Chip-Scope pro debugging tool. The presence of the controller increases the lifetime and safety of the battery cell pack. By continuously monitoring the battery voltages and currents, systems are protected from malfunctioning or damage due to voltage/ current changes.

Keywords: *Battery Monitoring System, UART, Xilinx ise 14.4, FPGA, Chip-Scope Pro*

Introduction

Approximately 71% of surface of the earth is occupied by sea is still people does not know about the deep sea completely due to the water pressure is increasing 1 atmospheric pressure per every 10m diving. Further various studies about the ocean such as marine environment, submarine earthquake, ocean life, marine resources research etc are need to carried out. In this regard Autonomous Underwater Vehicles (AUVs) have a wide range of applications in marine geosciences, and are increasingly being used in the scientific, military, commercial, and policy sectors. They are having subsystems like propulsion, communication mechanical,

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electrical and power etc. Battery Management System (BMS) in autonomous underwater vehicle (AUV) not only measure the important parameters of the battery packs such as current, voltage, and temperature, and also estimate the state of charge (SOC) of battery packs. Power requirement n AUV is very much supplemented with the help of Li ion cells(J. Kimura and H. Shibasak,1995).The Li ion cell batteries are placed in an aluminum frame for easy removal. Power diodes are connected between batteries to prevent them charging each other batteries and also ensure toeven discharge. Each battery connected to a power distribution board attached to the aluminium frame(H. S. Nalwa,2003). A charging port on the power board provides convenience by allowing the batteries to be charged without their removal from the lower hull as shown in Figure 1.

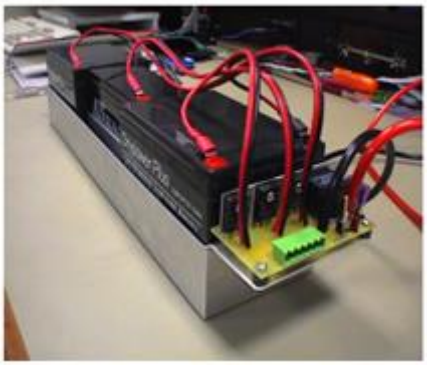

Figure.1. Li ion Cell Batteries housed in Al Hull

Li-Ion batteries are the better option because of compact size and long life. Lithium-ion battery has many other merits as shown in Figure 2. than other batteries such as high operating voltage, very high energy density, maintenance free,safety, no gas emittance while charging and is longer life-time(C. D. Scott and R. E. Smalley,2003).

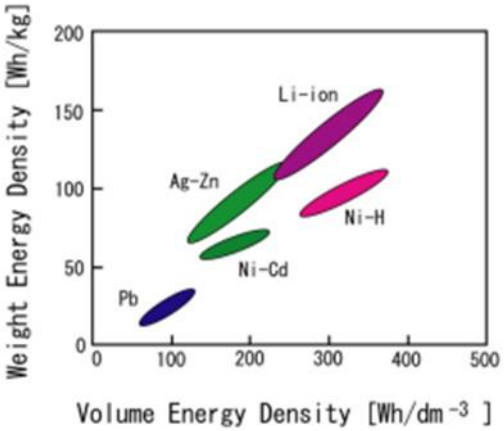

Figure 2. Volume Energy Density vs Weight Energy Density of Several Batteries

Proposed Method

In underwater applications as the batteries are the main source of power to various subsystems such as instrumentation system and on board computer etc. To ensure the reliable operation of all other subsystems, they should be operated with constant voltage irrespective of external operating conditions. BMS is an electronic system that monitors the rechargeable Li-Ion battery consisting of nine cells, and total output voltage/current is delivered to respective sensors. If these parameters are within the limit , it will switch on the battery

otherwise BMS will switch off the output using relay. The basic block diagram of FPGA based Battery monitoring system is shown in the Fig.3. It contains 9 cell Li-Ion battery pack, voltage and current sensors, Analog to Digital Converter(ADC), FPGA, relay and PC. To acquire the parameters of the battery cells, Sigma-Delta Analog to digital converter(ADC) is employed in the battery monitoring system. ADC communicates to the BMS controller using SPI protocol. The SPI sends the converted data to the controller in a serial line with clock synchronization(Ching-Kuo Wang, Sheng Chen and Han-Pang Huang,2007). The data from the FPGA controller is then sent to onboard PC with RS-232 standard. The BMS controller implemented in FPGA consists of ADC interfacing module and UART. FPGA is interfaced to ADC which can take the analog data from the current and voltage sensors converts into digital data. Digital data read by the BMS controller from ADC is also transmitted to PC with RS-232 standard. In this work BMS controller is implemented in FPGA hardware using verilog HDL (Volnei A.Pedroni,2007)

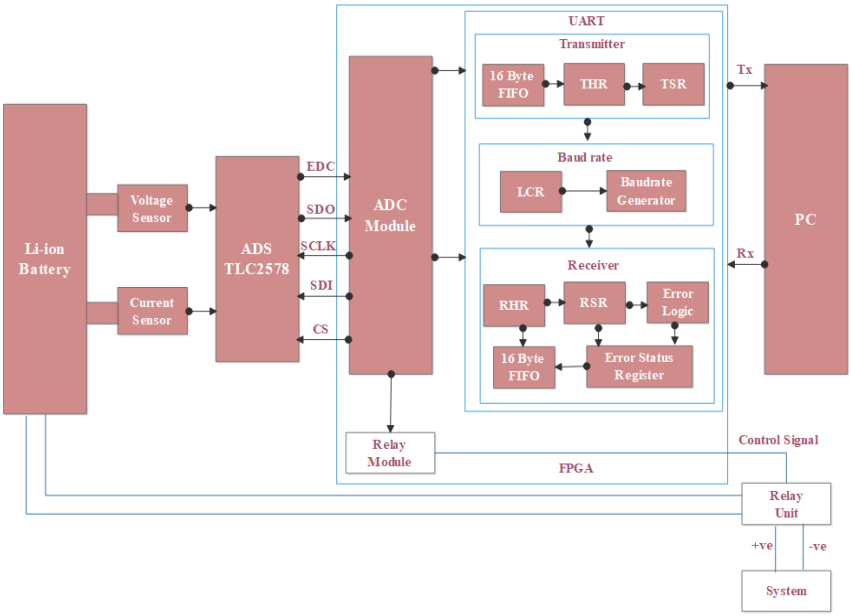

Figure 3. Block Diagram of BMS Controller System

BMS Controller

BMS Controller implemented in this paper consist of two modules ADC interfacing module, UART. ADC interface module is used for communication between ADC and UART with SPI Protocol. The Serial Peripheral Interface (SPI) standard specifies a synchronous serial interface in which data is shifted in or out from a serial peripheral device one bit at a time. SPI communicates with controller is having five signals such as EOC, SDI, SCLK, SDO, CS shown in Figure 3. Controller communication is initiated with four signals (Charles H. Roth, Jr,2007). Chip Select (CS) is to enable the serial port and is controlled by the controller. It goes low at the start of transmission and returns high at the end of transmission. Serial Clock (SCLK) is the serial port clock provides the timing of the serial communication and is controlled by the controller. Serial Data Input (SDI), transfers data serially into the ADC device and data values are latched on the rising edge of the SCLK. Serial Data Output (SDO),

transfers data serially out of the slave device and data is shifted out on the falling edge of the SCLK.After receiving the initialization and conversion commands from FPGA, ADC starts analog to digital conversion and sends the converted data to the UART controller. UART consist of three blocks transmitter, baud rate generator, and receiver (Zoran Salcic and Aslm Smallagle,2007).

In case of Asynchronous transmission, Start Bit is added to the data. It is an 8-bit UART, which consist of start bit, stop bit and parity bit. Transmitter block consist of three sub modules 16-byte FIFO, Transmitter Hold Register(THR) and Transmitter Shift Register(TSR). The Baud rate generator block consist of two sub modules Line Control Register(LCR) and baud rate generator. The Receiver block consist of five sub modules Receiver Hold Register(RHR), Receiver Shift Register(RSR), Error Logic , Error Status Register(ESR),16-byte FIFO. It operates at 10MHZ of baud clock.

Implementation

The controller consists of two modules ADC interfacing module and UART are realized in Verilog HDL, simulated in modelsim DE10.1d. and implemented in Spartan 5M FPGA board. Debugging is performed in chip scope pro 10.1 version andXilinx ISE 14.1. ADC interfacing module will establish the communication between ADC and UART. UART module generates the bits and transmit the data collected from controller to onboard PC. ADC interfacing module is based on the sampling time. Whenever chip select(CS) signal goes low, then SCLK signal sent to ADC and initialize conversion operation. For every falling edge of the SCLK, ADC receives the commands from the Host and send the converted data to the Host. Here EOC goes from high to low at the end of the sampling and remains low until the conversion is completed and data is ready. The entire operation is represented in state diagram as shown in Figure 4.

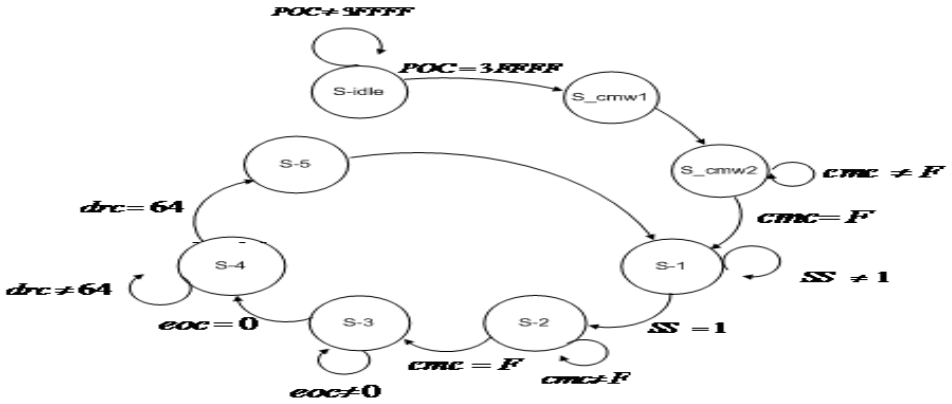

Figure 4.State diagram of ADC interfacing module

When power is on, if the reset signal is ‘1’, then the system is in idle state. If the reset is ‘0’ then it enters into the states S-cmw1 and S-cmw2, and then it enters into the state 1. Then goes to the next state i.e.S-2, where ADC samples the selected Analog Signal according to the command then analog data is converts into digital data and goes to the state S-3. If it is over then EOC (end of conversion) signal is low. Then goes to the states S-4, S-5. In this state digital data is send to the FPGA after receiving the data it again enters into state 1. This process will repeats again and again for every 100 msec. To receive the error free data, UART is implemented with status register as shown in Figure.5.

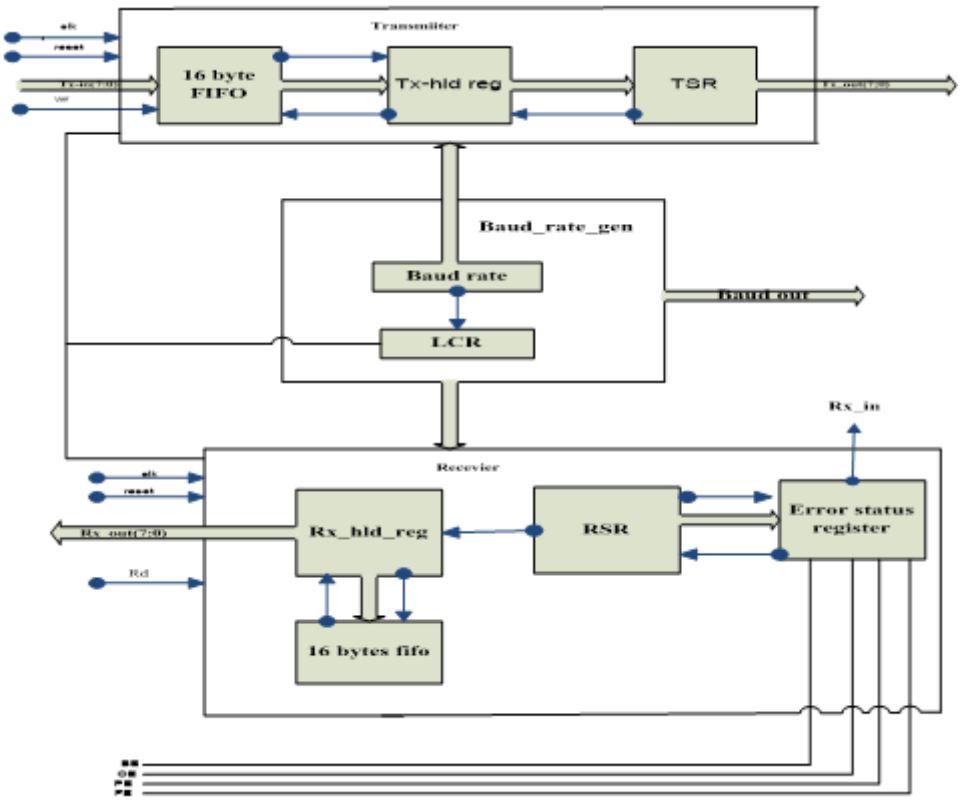

Figure 5. UART Architecture with status registers

UART Transmitter: 8-bit data TXIN (7:0) is applied to the input of the transmitter. From the input pin data is sent to FIFO. When WR is high and FIFO is full, it sends signal to 8-bit Transmitter Hold Register(THR). At the same time, if 12-bit Transmitter Shift Register(TSR) is empty sends signal to THR that is ready to receive bits from TSR which is an 12-bit register in which framing occurs.If transmitter bit is high then it will go to next state the X-start, otherwise it will stay in the same state. If bit cell count 16 is then it will go to the next state X-wait. If bit cell count is 15 then it will go to the next state X-parity else state X-wait. If bit cell count is not equal to 15 then it will go to the state X-stop. If shift enable is 0, then it will go to the state X-shift. If shift enable is 1, then it will go to state X-wait. If bit cell count is 1 then it go to the Idle state as shown in Figure 6.

Figure 6. State diagram of UART transmitter

Baud Rate Generator consist of Line control register shown Figure 7. is a byte register, used to transmit the data .The frame consist of parity bits, stop bits, baud rate selection and word length can be changed by writing the appropriate bits in LCR as shown in Table.1, format of which is show selection lines for selecting different baud rates, odd/even parity and data word length.

Bit	**VALUE**			**Description**
	BIT0	**BIT1**	**BIT2**	**Baud rate Selection**
0,1,2	0	0	0	57600
	0	0	1	38400
	0	1	0	19200
	0	1	1	9600
	1	0	0	4800
	1	0	1	2400
	1	1	0	1200
	1	1	1	600
3	0			Even Parity
	1			Odd Parity
4	0			Parity Disable
	1			Parity Enable
	BIT4	**BIT3**	DW Length	

5,6	0	0	5
	0	1	6
	1	0	7
	1	1	8
7	0		1 stop bit
	1		2 stop bit

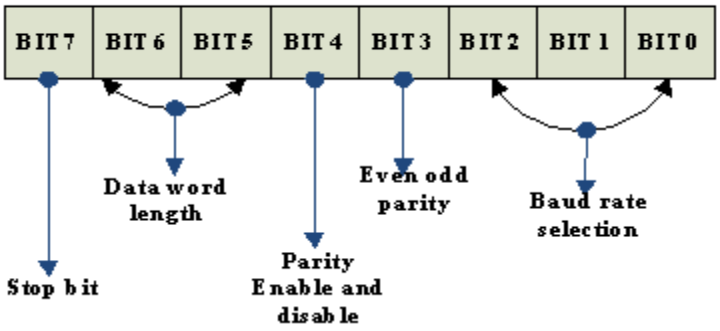

Figure 7. LCR format

UART Receiver

The output from the transmitter is sent to the receiver as input. All the bits send to the 12 bit Receiver Shift Register (RSR), serially one by one until the entire frame is stored. If the Receiver Hold Register (RHR) is empty, it sends signal to RSR so that only the data bits from RSR goes to 8 bit RHR. The remaining bits in the RSR are used by the error logic block. Receiver FIFO send the signal to RHR so that the data bits goes to FIFO. The operation of receiver is implemented using state diagram shown in Figure 8.If recdata is 0 it go to next state R-center,other wise it will stay in same state. If bitcellcount is not equal 1 and recdata is 0,then it will go to next state R-wait. If bit cell count is 15, then it will go to the next state R-sample. If Shift&count is 0 then it will go to next state R-stop. If Count is 8, then it will go to next state R-start.

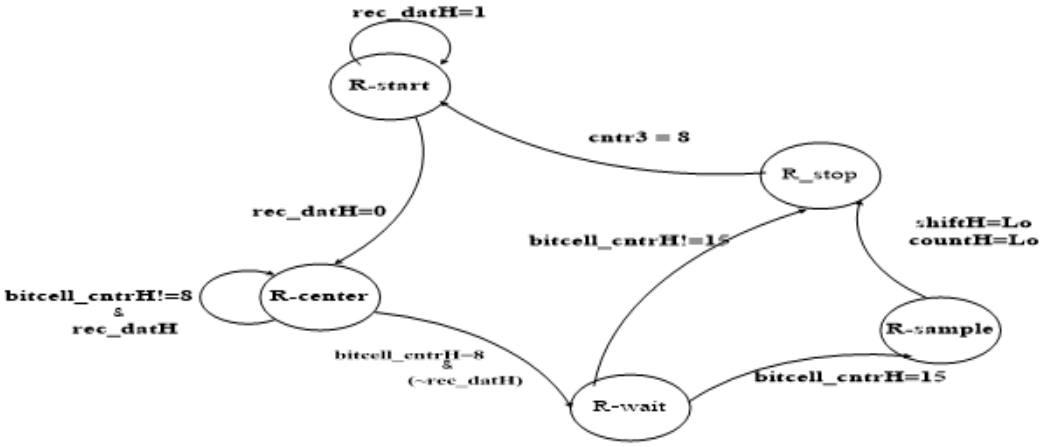

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Figure 8. State diagram of Receiver.

Results and Conclusions

BMS controller consists of UART and ADC interface modules are designed using sequential state machines are realized in verilog . Figure 9. shows the RTL of a controller consists two modules. The functional simulation of these blocks are carried out modelsim simulator. The modelsim results of BMS controller and its subblocks UART communication and ADC interfacing are shown in Figure. 10-11 respectively. For simple reorganization here transferred the eight bit data 10100101 to PC from FPGA with error elimination. After implementation in FPGA it was validated against chipscope pro. Similarly BMS controller s validated using chip scope pro logic analyser an the results of ADC interfacing and UART are shown in Figure. 12 (a) and (b) respectively.

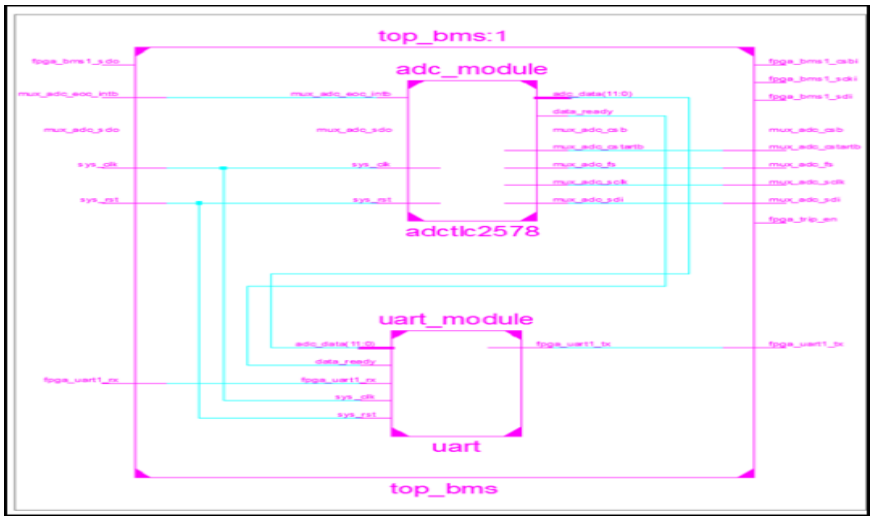


Figure 9. RTL schematic of BMS

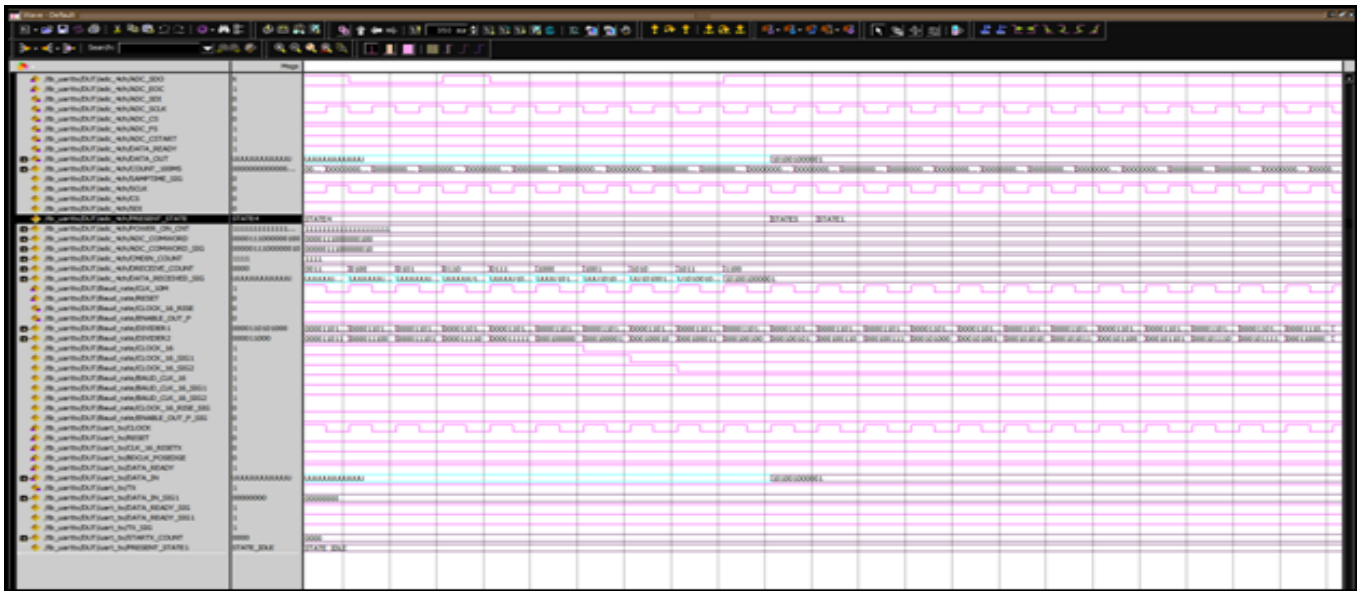
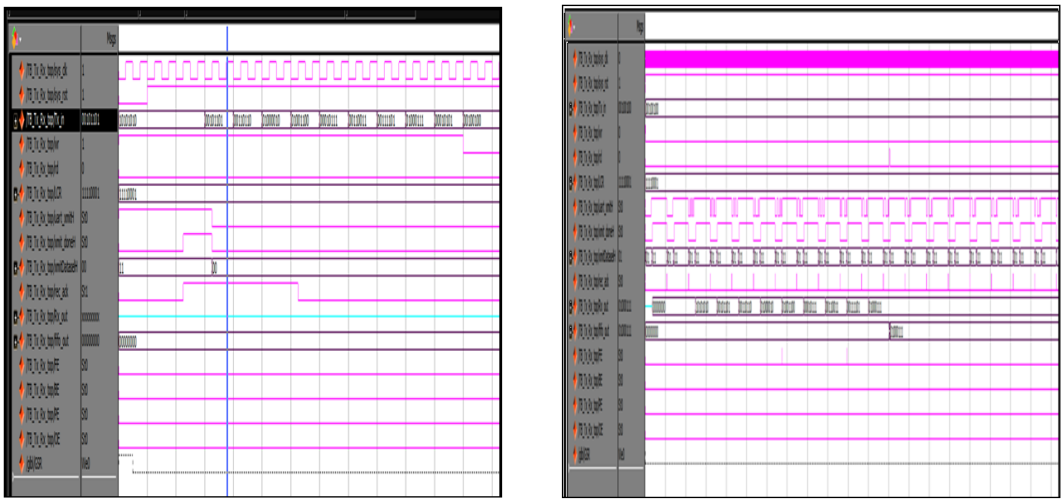
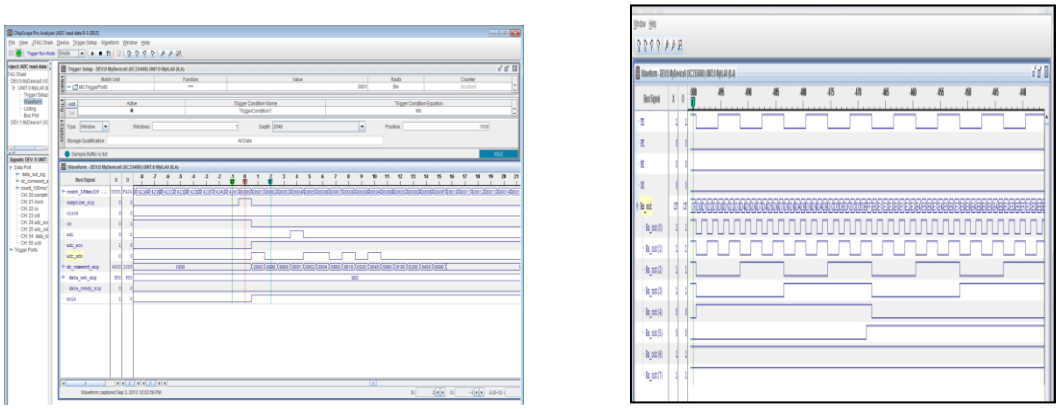


Figure 10. Simulation Results of BMS Controller



(a)UART Transmitter (b) UART Receiver

Figure 11.Simulation results



(a) ADC interfacing Circuit Results (b) UART Results

Figure12. Validation Results of BMS Controller in chip-scope pro

Conclusion

This paper thoroughly discussed about design and implementation of controller for battery monitoring system using FPGA. As compared to the existing systems the proposed system hardware has the advantages such as low power consumption, low cost, by using the FPGA which leads to high integration. It finds the applications in Electric and Hybrid electric vehicles, High power portable equipment, backup Battery systems etc. This design can help to observe the internal condition of the battery and also serve for different baud rate requirements of input and output. Hence the FPGA is a better option for data acquisition system and all these parameters are stored in the memory.

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