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Research Article

A Systematic Review and Research of Energy Efficient Evaluation in WSNs

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Abstract

This research provides a blueprint for the energy efficient assessment of sensor node architectures with a couple of low-end processors and radio as well as a couple of high-ended, high-end energy-performance processor and radio systems and includes the methodologies and techniques for the assessment of power efficiency in WSNs. The presentation of an interface for a coprocessing device dynamically reconfigurable for a wireless sensor node. The hardware accelerator is tailored to manage sensor data streams which cannot be managed effectively by micro-controllers with low power. The use of reconfigurable computing mechanisms achieves high energy efficiency. The design specifics involve many, specialized and reconfigurable processing steps. The size of the reconfiguration data is reduced using several reconfiguration levels for a fast and efficient dynamic reconfiguration.

The second document describes that such nodes may provide a highly dynamic range of applications from basic temperature measurement collections or motion sensing to advanced sensor data signal processing. Our model discusses trade-offs in energy efficiency in connection with which processor and radio to select for each mission. To do this we have a general Semi-Markov Decision model, one with dynamic and one with static interconnect, to optimize the asymptotic existence of two alternative designs. The resulting models are simulated and implemented in the measurements recorded on an existing two-radios platform and two processors. Our findings demonstrate how the benefits of such a system can be quantified for each component's energy consumption properties. Moreover, on the basis of our power budget estimate, we infer that, considering the energy overhead of such systems, the conception of a reconfigurable link between multiple processors and radios would result in efficiency gains.

A definition of periodic dynamic reconfiguration of a limited heterogeneous data path may lead to suitable device solutions for the target domain. To respond, the effect of the overhead reconfiguration on the overall effectiveness of the device is closely observed. Our tests therefore demonstrate the low energy consumption obtained in processors and ASICs, the low reconfiguration overhead and the particular architectural area in the design space.

The case study from certain papers has demonstrated that the heterogeneous cluster architecture expands the conventional parallel processor cluster with an IPA accelerator. Although programmable processors ensure programming that is legacy for simple peripherals management,

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the download of the data-intense and control-intensive kernels to the IPA can lead to substantially higher device level performance and energy efficiency.

1. Introduction

In silicon technology and computing architectures continuous developments are the main elements that enable the development of modern smart systems. Improved computing power opens the door for meaningful devices, agrees on specific algorithms and operates on the physical world. The wide range and low power consumption of such systems make it easy for end users to deploy them on a large scale. Modern cloud architectures provide edge CPS so that computational resources can be spread more flexibly, and the distance can be narrowed in applications involving fast real-time computation. Mechanisms are used to promote the connection between the edge nodes and the centre of the data centre. Public cloud services, for example, provide specialized APIs, dedicated applications to program and control edge machines and to download activities.

Video monitoring represents an existing application area that addresses Cloud infrastructure both in its edge and in its heart. The energy efficiency of camera sensors at any level is mandatory when it comes to traffic control applications. Although they demand high volumes of data that further raise radio energy requirements, it is important to minimize energy consumption as camera sensors come mainly from renewable energies and small batteries. Similarly, energy-efficient motors in the DC centre are also needed for any point of the architecture. For example, if the camera sensors detect such events, the video transmission is transferred to the DC core where more powerful algorithms are used to analyse the events. When camera sensors sense particular events, for example, video streaming goes to the DC heart, which uses more efficient algorithms to interpret events.

For many highly embedded near-sensors processing devices, including wireless sensor networks, the wearable end-nodes of internet, high performance and intense energy consumption are the strict criteria. One of the more traditional methods of improving the energy performance of highly embedded computer systems is through integrating spatial heterogeneity with application- or domain-specific accelerators in a single machine fabric. In the other hand, the latest ultra-low power architectures run on many homogenous, near-threshold programmable processors. A parallel approach to low-voltage computing has been developed to add high energy efficiency to output scalability.

Hardware that is configurable is seen to be more starving than microcontrollers with low power and is thus not commonly used for WSN applications. However, when implementing such challenging networking activities, FPGAs allow dramatically higher reliability and energy efficiency. In addition, they are very promising candidates for general purpose nodes because their functions can be reprogramed before or after use. In this paper the most commonly used WSN Routing Protocol on modern FPGAs will provide a novel implementation. This is the first solution to our understanding and our studies show that quick routing decisions are taken at very low energy costs. We implemented GPSR on two separate Xilinx FPGA units to measure the reliability and energy usage in a real environment and compared them with an analogous software application on a power-low Intel Atom CPU to measure their output in an optimized environment. Our experimental findings indicate that the method proposed is more than 31 times more efficient in executing the GPSR protocol and consumes more than 90% less energy than the software solution. Moreover, these gains appear to be substantial in contrast with advanced low-power CPUs, based on our figures.

2. Methodology and Techniques used to Evaluate Energy Efficient

This paper is explained about the methodology and techniques which are used in the Energy Efficient platform of WSNs. The main platform is Traffic Monitoring Platform which has Reconfigurable Antennas, Image Processing Acceleration and Energy Harvester.

a) Traffic Monitoring Platform

The architecture has three major features to enable image processing at the edge and in the DC core.

i. A power machine with an ultra-low power sensor.
ii. A sophisticated subsystem for radio communication directly related to the ULP.
iii. A remote server designed to accelerate complex image processing operations with an FPGA board. A terminal between the ULP and the remote server is also placed. This latter is designed to receive and transmit data from ULPs through a regular wired connection to the remote server. In order to facilitate connectivity in areas which are not reached by wireless infrastructures, wireless communication is necessary. It also encourages the use of many nodes to reach broader geographical regions.

The ULP is fitted with a machine solution for high energy efficiency. To this end, the device integrates a powerful microcontroller for general purposes with many DSPs and hardware accelerators. In specific, the sporting hardware blocks are used to facilitate the execution of the CNNs that are in turn used to process images acquired. The remote server also comes with a devoted FPGA accelerator that incorporates personalized CNN processing pipelines. This was synthesized successfully by focusing upon the production and testing of an HLS toolkit. It is only via the contact protocol that you can support the ability to customize the radio communication subsystem. WiFi is a candidate for low power consumption at high transmission speeds. However, regular implementation of such protocols offers a protected gap that is not necessarily appropriate for actual implementations, including road traffic surveillance. Modulation schemes containing multiple transmitters and multiple receivers are used to address this limitation; however, the power usage of such solutions renders them impossible for boundary applications.

In general, a device that includes a reconfigurable directive antenna has a typical (omnidirectional) energy efficiency advantage. The transmitting power is decreased by a certain received signal power. The device then transfers data with less energy without changing the communication efficiency. Conversely, the obtained signal energy is higher given a certain power of the transmitted signal. As a result, the device will relay data on a longer distance at higher speeds. Again, less energy is required so the data can be transmitted in a shorter duration.

b) GPSR Routing Scheme

This section describes the Greedy Perimeter Stateless Routing (GPSR) protocol that involves two different methods for the forwarding of network packets. Each network node which supports the GPSR Protocol must maintain a table with the necessary information, effectively on the location and addresses of all single-hop radio neighbours. The table contains all the necessary information needed for forwarding decisions. The packet headers of GPSR have a flag that indicates whether the packet's mode is gullible or perimeter. Initially, each data packet is labelled as greedy on its source. Packet sources also include in the accompanying fields the geographical position of the destination. In the GPSR system, a node initially looks for the node that is geographically closest to the destination as it receives a hedge-mode packet for forwarding. Then the packet is sent to the node, which is the better alternative locally. This definition is extended to

each node before it reaches the destination. Packets in perimeter mode are forwarded with a plain flat graph. The key reason we want to incorporate GPSR is that it is undoubtedly the most used protocol, primarily because of its low message complexity. The protocol is the most frequently used protocol and extremely robust packet delivery on densely deployed wireless networks. Furthermore, since a routing protocol such as GPSR, which does not enable each node to have a global network state, has relatively small memory capacity, it is very much in line with the FPGA's functions.

The Greedy Forwarder module uses the greedy algorithm which determines the shortest path for the data packet it receives and transmits it to the nearest node. This subsystem's design is seen. It consists mainly of the Euclidean Distance Metric part, which determines the shortest path between all the nodes of the nearby table, as well as some basic modules, which specify the next hop and whether the packet should stay in the greedy mode or be modified to the perimeter one.

c) Reconfigurable Function Unit

Rapid dynamic reconfiguration of RFU operators, memory blocks and interconnecting structures are an important part of standard RFU process execution such that certain hardware tools can be flexibly re-used in any clock cycle to execute various calculation steps. In addition, the full RFU to carry out separate tasks sequentially over time is reused by dynamic reconfiguration. A new reconfiguration mechanism was used to provide a comprehensive explanation for this quick and effective intra-task and inter-task reconfiguration. The RFU's 426 configuration bits are essentially reconfigured in one task by partial multi-context swaps and causes no latency. There is a small multi-context table (MCT) for each data path component specifying their own setup. In every clock cycle and for every variable, various configurations can be selected simultaneously. A central tag signals all MCTs and thus stipulates the existing RFU setup and synchronizes the background range. This tag signal is generated in the RFU run control unit from a reconfigurable table (named MPT). The MPT specifies tag sequences (including loops and jumps), which defines RFU for each clock cycle of a long RFU operation.

The processor may use two methods to invoke RFU operations: The Single-cycle execution (ESR), which addresses a specific tag in the MPT and selects a specific configuration for a single computation stage, will initiate a single process. The multi-cycle execution instruction can be used to trigger longer operations. The RFU run control unit uses the MPT knowledge for a predefined series of computation processes in such a multi-cycle operation. The RFU is thus completely autonomous in carrying out an EMR instruction. Its life will vary from 2 to 100 cycles before an entire mission has been carried out with a single EMR order. Intra-task reconfiguration for a software engineer is basically straightforward under the ESR and EMR instructions.

d) Dynamically Reconfigurable Architecture

The architecture was built with generic and modular components to allow for high levels of VHDL customization. This allows the entire functional unit to be modified for such arithmetical operations. Frequency domain filtration and transformations primarily involve multiplication and aggregation of integer, with forward error correction and encryption algorithms focused mainly on finite field arithmetic. Two related units have some benefits for these algorithms: Filtering and encryption can also be carried out by functional units pipelined at algorithm level. The computing processes are parallel. A single stage will only lead to a gain in area with the use of integer and finite field arithmetic’s with reconfigurable units while the tank architecture eliminates energy

demand globally and improves speed. A series of advanced processing units operating as anti-machines bases the coprocessing unit. The configuration controller named Configuration Manager controls each key processing block, later, called level.

3. Conclusion

This article discusses how the WSNs assess productivity methods and methodology. Reduced overhead configuration allows for a quick dynamical reconfiguration of the processing phases while allowing over-the-air delivery of new wireless sensor network configuration results. A test scenario was identified for the proposed architecture and promising results were drawn. Improving the generation of tag sequence in the CM by input from the process would allow more flexibility in algorithm implementation and data dependency support.

Another argument is that in a case study the idea of regular dynamic reconfiguration was explored. The rough granularity and heterogeneity of the RFU provided the desired high energy efficiency and kept the design compact and scalable with dynamical reconfiguration. Our RFU differs from other architectures by how fast dynamic reconfiguration has been used successfully to extensively reuse heterogeneous Data Path tools.

This paper introduces a different approach to machine heterogeneity, which improves the strength of the Purple multicore cluster with ultra-low reconfigurable acceleration. Architectural heterogenicity is a powerful approach to improving the energy profile of computer systems based on studies incorporating IPA into the PULP platform. As it has been demonstration of that, it is a very successful solution both for energy usage and bandwidth assisted, and the routing protocol can be also altered in real time when necessary, We assume this paper has been used for the first time in a WSN environment in network tasks for reconfigurable networks, and may well initiate a new architecture strategy for the future extremely challenging WSN nodes.

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